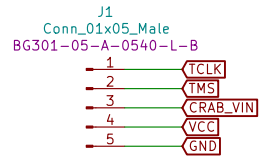
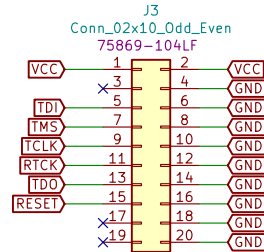


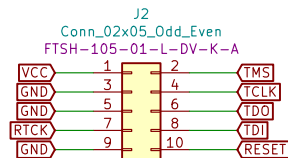
## CRAB INTERFACE



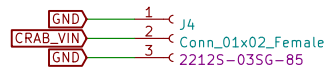
## ARM 20-PIN INTERFACE



## ARM 10-PIN INTERFACE



## POWER



### JTAG Interface

ARM 10-PIN Interface				ST 14-PIN Interface				OCD5 16-PIN Interface				ARM 20-PIN Interface			
VCC	1	2	TMS	JEN	1	2	/RESET	TMS	1	2	VCC (optional)	VCC	1	2	VCC (optional)
GND	3	4	TCLK	TDI	3	4	TESTAT	CPUGLK	3	4	GND	TDI	3	4	GND
RTCK	5	6	TDO	VCC	5	6	RESET	TDI	5	6	RESET	TMS	5	6	GND
GND	7	8	TDI	TMS	7	8	TDI	TRST	7	8	GND	RTCK	7	8	GND
GND	9	10	RESET	TCLK	9	10	TRST	TRAP	9	10	GND	RESET	9	10	GND
				TDI	11	12	TDI	TRAP	11	12	GND	TDI	11	12	GND
				TDI	13	14	TRST	TRAP	13	14	GND	TDI	13	14	GND
				TDI	15	16	TRST	TRAP	15	16	GND	TDI	15	16	GND
				TDI	17	18	TRST	TRAP	17	18	GND	TDI	17	18	GND
				TDI	19	20	TRST	TRAP	19	20	GND	TDI	19	20	GND

Signal	Connects to...
TMS	Test Mode State pin — Use 100K Ohm pull-up resistor to VCC.
TDO	Test Data Out pin.
RTCK	JTAG Return Test Clock. (see Note below)
TDI	Test Data In pin — Use 100K Ohm pull-up resistor to VCC.
TRST	Test Reset/ pin — Use 100K Ohm pull-up resistor to VCC. TRST is optional and not available on some devices. You may leave it unconnected. This is an open-collector/open-drain output.
TCLK	Test Clock pin — Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage — Power supply for JTAG interface drivers.
GND	Digital ground.
RESET	RSTIN/ pin — Connect this pin to the (active low) reset input of the target CPU. This is an open-collector/open-drain output.
CPUGLK	CPU clock (according IEEE Standard 1149.1).
OCDSE	Enable/Disable OCD5 interface (Infineon-specific).
TRAP	Trap condition (Infineon-specific).
BRKIN	Hardware break in (Infineon-specific).
BRKOUT	Hardware break out (Infineon-specific).
/JEN	JTAG Enable (STMicroelectronics specific).
TESTAT	JTAG ISP Status (STMicroelectronics specific) (optional).
/RST	Chip reset (STMicroelectronics specific).
/TERE	JTAG ISP Error (STMicroelectronics specific) (optional).

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